OIPE IAP48
SEP 22 2006
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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended): An apparatus for use in performing a floating point multiply-accumulate operation, comprising:

a plurality of latches that contain a plurality of exponents of operands for the operation;

a carry-save adder, coupled to the latches, that receives the exponents of operands and performs a carry-save add operation on the exponents of operands to produce a first result;

a control circuit for generating a control signal; and

a logic block, coupled to the carry-save adder, that receives the first result and performs a carry-lookahead add operation on the first result to produce a second result, the logic block having a logic circuit that performs an exclusive-OR logic operation between a most significant bit of the second result and the control signal to produce a value for use in the floating point multiply-accumulate operation.

2. (currently amended): The apparatus of claim 1, wherein the logic circuit includes a ~~redundant~~ logic stage for processing said most significant bit in the logic block.

3. (original): The apparatus of claim 2, wherein the redundant logic stage performs the logic operation on the most significant bit in parallel with at least a portion of the carry-lookahead add operation.

4. (original): The apparatus of claim 1, wherein the logic circuit performs the logic operation to produce a shift value for use in the floating point multiply-accumulate operation.

5. (cancelled).

6. (currently amended): ~~The apparatus of claim 5, wherein the control circuit generates the control signal~~ An apparatus for use in performing a floating point multiply-accumulate operation, comprising:

a plurality of latches that contain a plurality of exponents of operands for the operation;

a carry-save adder, coupled to the latches, that receives the exponents of operands and performs a carry-save add operation on the exponents of operands to produce a first result;

a control circuit for generating a control signal based upon a Single Instruction Multiple Data operation; and

a logic block, coupled to the carry-save adder, that receives the first result and performs a carry-lookahead add operation on the first result to produce a second result, the logic block having a logic circuit that performs an exclusive-OR logic operation between a most significant bit of the second result and the control signal to produce a value for use in the floating point multiply-accumulate operation.

7. (currently amended): The apparatus of claim 1 ~~5~~, wherein the control signal is a pair of complementary signals and wherein the control circuit generates the pair of complementary signals.

8. (original): The apparatus of claim 1, wherein the logic block includes a carry-lookahead adder having complementary logic circuits for providing complementary outputs as the second result.

9. (currently amended): A method for use in performing a floating point multiply-accumulate operation, comprising:

receiving a plurality of exponents of operands for the operation;

performing a carry-save add operation on the exponents of operands to produce a first result;

performing a carry-lookahead add operation on the first result to produce a second result;

generating a control signal;

receiving ~~a~~ the control signal; and

performing an exclusive-OR logic operation between a most significant bit of the second result and the control signal to produce a value for use in the floating point multiply-accumulate operation.

10. (currently amended): The method of claim 9, wherein the performing the logic operation step includes using a ~~redundant~~ logic stage for processing said most significant bit in a carry-lookahead adder circuit.

11. (original): The method of claim 10, wherein the using step includes processing the most significant bit in parallel with at least a portion of the step of performing the carry-lookahead add operation.

12. (original): The method of claim 9, wherein the performing the logic operation step includes producing a shift value for use in the floating point multiply-accumulate operation.

13. (cancelled).

14. (currently amended): ~~The method of claim 13, wherein the generating step includes generating the control signal~~ A method for use in performing a floating point multiply-accumulate operation, comprising:

receiving a plurality of exponents of operands for the operation;

performing a carry-save add operation on the exponents of operands to produce a first result;

performing a carry-lookahead add operation on the first result to produce a second result;

generating a control signal based upon a Single Instruction Multiple data operation;

receiving the control signal; and

performing an exclusive-OR logic operation between a most significant bit of the second result and the control signal to produce a value for use in the floating point multiply-accumulate operation.

15. (currently amended): The method of claim 9 ~~13~~, wherein the generating step includes generating a pair of complementary signals as the control signal.

16. (original): The method of claim 9, wherein the performing the carry-lookahead add operation step includes using complementary logic circuits for the carry-lookahead add operation to provide complementary outputs as the second result.

17. (new): An apparatus for use in performing a floating point multiply-accumulate operation, comprising:

a plurality of latches that contain a plurality of exponents of operands for the operation;

a carry-save adder, coupled to the latches, that receives the exponents of operands and performs a carry-save add operation on the exponents of operands to produce a first result;

a control circuit for generating a control signal; and

a logic block, coupled to the carry-save adder, that receives the first result and performs a carry-lookahead add operation on the first result to produce a second result, the logic block having a logic circuit that performs an exclusive-OR logic operation between a most significant bit of the second result and the control signal to produce a value for use in the floating point multiply-accumulate operation,

whereby the apparatus forms the floating point multiply-accumulate operation using a single carry-save adder (CSA).